*R20 Regulation* *Subject code:3P6DD*

# TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

## B.Tech VI Semester Supplementary Examinations, May 2025

## VLSI DESIGN

## *(ECE)*

***Maximum Marks: 70*** Date: 23.06.2025 Duration: 3 hours

**Note:** **1.This question paper contains two parts A and B.**
**2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.**
**3. Part B consists of 5 Units. Answer any one full question from each unit.**
**4. Each question carries 10 marks and may have a, b, c, d as sub questions.**

Part-A

| All the following questions carry equal marks (10X2M=20 Marks) | | Marks | CO | BTL |
|---|---|---|---|---|
| 1 | What is Moore's Law. | 2M | 1 | L1 |
| 2 | Define Threshold voltage. | 2M | 1 | L1 |
| 3 | List the various color coding used in stick diagram. | 2M | 2 | L1 |
| 4 | List the advantages of scaling. | 2M | 2 | L1 |
| 5 | Define Risetime. | 2M | 3 | L1 |
| 6 | Define fan out. | 2M | 3 | L1 |
| 7 | Why is barrel shifter very useful in the designing of arithmetic circuits? | 2M | 4 | L1 |
| 8 | Draw 2-bit comparator. | 2M | 4 | L1 |
| 9 | Implement Half adder using PAL. | 2M | 5 | L1 |
| 10 | What are functionality tests? | 2M | 5 | L1 |

Part-B

| Answer All the following questions. (5X10M=50Marks) | | Marks | CO | BTL |
|---|---|---|---|---|
| 11 | With neat sketches explain PMOS fabrication process. | 10M | 1 | L2 |
| | OR | | | |
| 12 | a) Explain NMOS inverter operation.<br>b) For nMOS inverter driven by another nMOS inverter, derive the expression for $Z_{pu}/Z_{pd}$ ratio. | 5M<br>5M | 1 | L2 |
| 13 | Sketch the circuit schematic, stick diagram and layout of CMOS 2-Input NAND gate. | 10M | 2 | L2 |
| | OR | | | |
| 14 | a) Explain about 2μm CMOS design rules for wires, transistors and transistors.<br>b) Write the demerits of Scaling. | 7M<br>3M | 2 | L2 |
| 15 | Explain in detail about Dynamic CMOS logic and CMOS Domino logic gates with suitable example. | 10M | 3 | L2 |
| | OR | | | |
| 16 | Describe three sources of wiring capacitance. | 10M | 3 | L2 |

| | | | | |
|---|---|---|---|---|
| 17 | Draw the basic circuit diagram of static RAM cell and explain its read and write operation. | 10M | 4 | L2 |
| | OR | | | |
| 18 | a) Design a four-bit parity generator using only XOR gates.<br>b) Draw the circuit diagram of carry select adder and explain it. | 5M<br>5M | 4 | L2 |
| 19 | Explain the architecture of CPLD with neat diagram. | 10M | 5 | L2 |
| | OR | | | |
| 20 | a) Write about CMOS testing.<br>b) Explain about design strategies for testing. | 5M<br>5M | 5 | L2 |



24